What is claimed is:

1. A nonvolatile semiconductor memory device, comprising:

a source region and a drain region that are mounted on a main surface of a semiconductor substrate and positioned at a specified distance from each other;

a channel region that is formed between said source region and said drain region;

a first gate that is provided above a channel region on a side toward said drain and via a first gate dielectric film; and

a second gate that is provided above a channel region on a side toward said source via a second gate dielectric film, wherein a lateral surface of said second gate is covered with a first dielectric film and an upper surface of said second gate is provided with a second dielectric film;

wherein said first gate is formed so as to cover said first gate dielectric film, the lateral surface of said first dielectric film, and the lateral surface of said second dielectric film; and wherein one end of said first gate is positioned on an upper end face of said second dielectric film.

2. The nonvolatile semiconductor memory device

according to claim 1, wherein said first gate is positioned with both ends placed in a gap region enclosed by said second gate and is filled so as to form a concave.

3. The nonvolatile semiconductor memory device according to claim 1, wherein the surface area of said first gate is A > B + C + D when the sidewall area within a gap region of said second gate is A, the bottom surface area within a gap region of said second gate is B, the flat surface area of the top of said second gate is C, and the sidewall area of the top of said second gate is D.

4. The nonvolatile semiconductor memory device according to claim 1, wherein said second gate controls a split channel formed within said semiconductor substrate via said second gate dielectric film.

5. The nonvolatile semiconductor memory device according to claim 1, wherein said second gate has a gate function for controlling both an erase gate and a split channel and acting as erase gate.

6. The nonvolatile semiconductor memory device according to claim 1, wherein said second gate dielectric film is the same as a gate dielectric film for a MOS transistor that composes a low-voltage section of a peripheral circuit formed on said semiconductor substrate.

7. The nonvolatile semiconductor memory device according to claim 1, wherein the material and film

thickness of said second gate are the same as those of a gate for a MOS transistor that composes a peripheral circuit formed on said semiconductor substrate.

8. A nonvolatile semiconductor memory device, comprising:

a source region and a drain region that are mounted on a main surface of a semiconductor substrate and positioned at a specified distance from each other;

a channel region that is formed between said source region and said drain region;

a first gate that is provided above a channel region on a side toward said drain and via a first gate dielectric film;

a second gate that is provided above a channel region on a side toward said source via a second gate dielectric film, wherein a lateral surface of said second gate is covered with a first dielectric film and an upper surface of said second gate is provided with a second dielectric film;

a third gate that is provided via a third dielectric film formed on said first gate;

a word line that is electrically connected to said third gate;

a contact hole that is made through a third dielectric film formed on said third gate; and

metal wiring that is connected to said word line via said contact hole;

wherein said contact hole is provided on a member having the same material and film thickness as a film that forms said second gate.

9. The nonvolatile semiconductor memory device according to claim 8, wherein said member is a polysilicon film.

10. A nonvolatile semiconductor memory device, comprising:

a first conductive well that is formed on a main surface of a semiconductor substrate;

a source region and a drain region that are formed in said first conductive well and positioned at a specified distance from each other;

a channel region that is formed between said source region and said drain region;

a first gate that is provided in a channel region on a side toward said drain and via a first gate dielectric film;

a second gate that is provided in a channel region on a side toward said source via a second gate dielectric film, wherein a lateral surface of said second gate is covered with a first dielectric film and an upper surface

of said second gate is provided with a second dielectric film; and

a third gate that is provided via a third dielectric film formed on said first gate;

wherein a bind region for binding a plurality of said second gates is provided on a region of said semiconductor substrate where an impurity diffusion layer including a second conductivity type is selectively formed.

11. The nonvolatile semiconductor memory device according to claim 10, wherein an impurity diffusion layer region including said second conductivity type is connected to said source region, said drain region, and a diffusion layer region of a select transistor for selecting said source region and drain region.

12. A method for manufacturing a nonvolatile semiconductor memory device having a memory cell array region and a peripheral circuit region, the method comprising the steps of:

forming a well region on a main surface of a semiconductor substrate;

forming a first gate dielectric film in said well region;

forming a first silicon film on said first gate dielectric film;

performing a line-and-space forming process for selectively patterning films including said first silicon film and said first gate dielectric film in said memory cell array region and forming a line region and a space region in a first direction;

forming a second gate dielectric film in said space region and forming a second silicon film in a region containing said second gate dielectric film;

patterning said second silicon film in such a manner as to extend said first dielectric;

forming an interpoly dielectric film in a region containing said second silicon film and forming a third silicon film for said interpoly dielectric film;

patterning said third silicon film and said second silicon film in a direction perpendicular to said first direction; and

patterning said first silicon film again;

wherein said second silicon film is patterned in the first direction so that an end of the resulting second silicon film pattern is positioned on said line region.

13. The method according to claim 12, wherein said first gate dielectric film is thinner than said second gate dielectric film.

14. The method according to claim 12, wherein said second gate dielectric film is formed after forming said

line and space, and forming a sidewall comprising a dielectric film on said first silicon film that is patterned in said memory cell array region.

15. The method according to claim 12, wherein a bind is formed by patterning said first silicon film in such a manner as to bind an end of a line formed in said first direction.

16. The method according to claim 12, wherein an impurity of a conductivity type opposite to that of said semiconductor substrate is introduced into said semiconductor region corresponding to the underside of said bind before said bind is formed.